

SN74LS139

Dual 1-of-4 Decoder/ Demultiplexer

The LSTTL/MSI SN74LS139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current – High			–0.4	mA
I _{OL}	Output Current – Low			8.0	mA

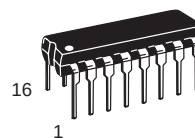


ON Semiconductor

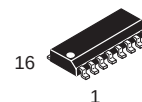
Formerly a Division of Motorola

<http://onsemi.com>

**LOW
POWER
SCHOTTKY**



**PLASTIC
N SUFFIX
CASE 648**



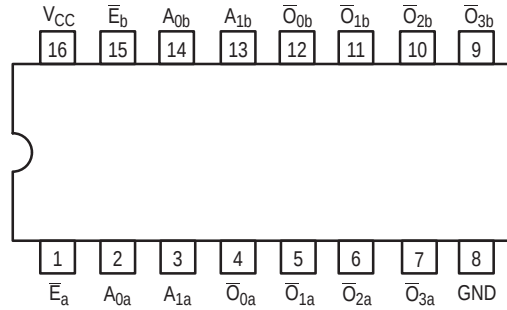
**SOIC
D SUFFIX
CASE 751B**

ORDERING INFORMATION

Device	Package	Shipping
SN74LS139N	16 Pin DIP	2000 Units/Box
SN74LS139D	16 Pin	2500/Tape & Reel

SN74LS139

CONNECTION DIAGRAM DIP (TOP VIEW)



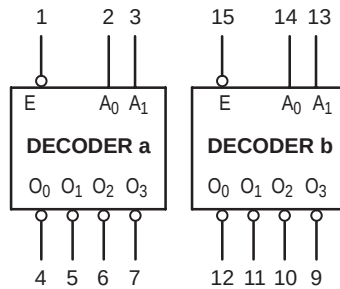
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
E	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\bar{O}_0 - \bar{O}_3$	Active LOW Outputs	10 U.L.	5 U.L.

NOTES:

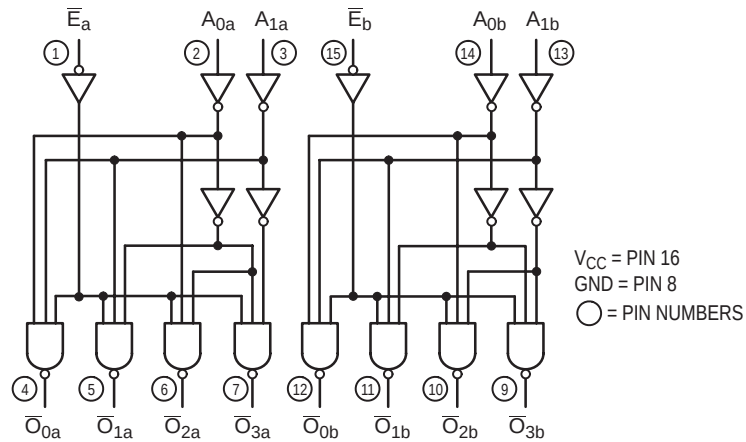
a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0 , A_1) and provide four mutually exclusive active LOW outputs ($\bar{O}_0$ – $\bar{O}_3$). Each decoder has an active LOW Enable ($\bar{E}$). When E is HIGH all outputs are forced HIGH. The enable

can be used as the data input for a 4-output demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\bar{E}$	A_0	A_1	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

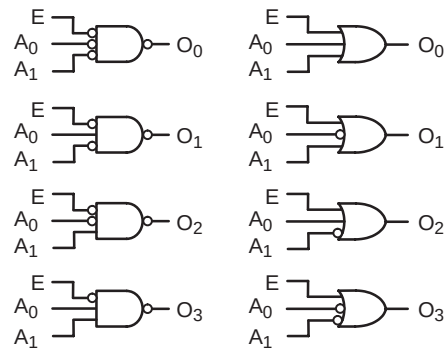


Figure a

SN74LS139

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			11	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Levels of Delay	Limits			Unit	Test Conditions
			Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay Address to Output	2 2		13 22	20 33	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay Address to Output	3 3		18 25	29 38	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	2 2		16 21	24 32	ns	

AC WAVEFORMS

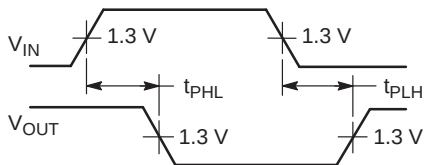


Figure 1.

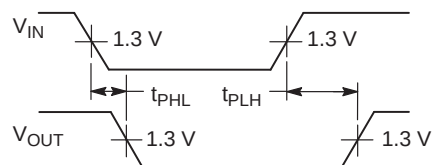


Figure 2.

